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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	**Application No.** 10/761,193	**Applicant(s)** JEONG ET AL.	
	Examiner DAVID P. RASHID	**Art Unit** 2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 September 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-9,14 and 15* is/are rejected.

7)☒ Claim(s) *6 and 10-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Amendments

[1] This office action is responsive to Response Under 37 C.F.R. § 1.116, After Final received on September 3, 2008. Claims 1-23 remain pending. Claims 1-15 remain pending.

Claim Rejections - 35 U.S.C. § 101

[2] In response to Amendments to Claims received on September 3, 2008, the previous § 101 rejections are withdrawn.

Claim Rejections - 35 U.S.C. § 112

[3] In response to Amendments to Claims received on September 3, 2008, the previous § 112 rejections are withdrawn.

Claim Rejections - 35 U.S.C. § 102

[4] The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

[5] **Claims 1-2** and **14** are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Pub. No. 2002/0012459 (published Jan. 31, 2002, hereinafter "Oh").

Regarding **claim 1**, *Oh* discloses a multi-layered real-time stereo matching apparatus (fig. 9a; fig. 12) comprising:

a left and a right image acquisition unit (“a camera for taking the scanning image…the other camera for taking the reference image” at ¶0004) for obtaining a left and a right image (“scanning image” and “reference image” at ¶0004; “reference image is taken from the viewpoint of the left eye, while the scanning image is taken from the viewpoint of the right eye” at ¶0002) of an object (“object” at ¶0005) on a spatial area (“an area enclosed by a solid line" at ¶0046 for both the reference and scanning image) from different positions (¶0004);

an image processing unit (the unit responsible for creating the digital images as disclosed by *Oh*) for converting the left and the right image to a left and a right digital image (fig. 9 are digital images); and

a multi-layered image matching unit (the processor responsible for execution of fig. 9b; “processor” at ¶0068), which includes a systolic array (“systolic array” at ¶0084; fig. 9; fig. 12), for comparing one scan line (R_1 at fig. 9b) in one of the left and the right digital image (“Reference Image” at fig. 9a) with multiple scan lines ($L_1 \ldots L_{64}$ at fig. 9b) in the other of the left and the right digital image (“Scanning Image” at fig. 9b) in real-time by using the systolic array so that each pixel in the one scan line matches another pixel in the multiple scan lines in the other digital image (“65th Calculation” at fig. 9b; ¶0084),

wherein said left and right digital images are left and right images of said object (“object” at ¶0005), and wherein matching the pixel in the one scan line with another pixel in the multiple scan lines enables location of the object in said spatial area (“an area enclosed by a solid line" at ¶0046 for both the reference and scanning image) so that the imprecision in location and

direction of, or distortion caused by, said left and right image acquisition unit is prevented (the purpose of *Oh* is to match the scanning and reference image due to imprecision in location and direction of the two cameras because they are both separate from each other in location and direction; *see* Response to Argument section).

Regarding **claim 2**, *Oh* discloses the apparatus of claim 1, wherein the multi-layered image matching unit (the processor responsible for execution of fig. 9b; "processor" at ¶0068) receives pixels of the one scan line (R_1 at fig. 9b) in the one digital image sequentially and receives pixels of the multiple scan lines ($L_1 \ldots L_{64}$ at fig. 9b) in the other digital image at a time, and calculates a disparity between one pixel in the one scan line and said another pixel in the multiple scan lines ("stereo disparity" at ¶0007).

Regarding **claim 14**, *Oh* discloses a multi-layered real-time stereo matching method (fig. 9b) , the method comprising the steps of:

(a) obtaining a left and a right digital image ("scanning image" and "reference image" at ¶0004; "reference image is taken from the viewpoint of the left eye, while the scanning image is taken from the viewpoint of the right eye" at ¶0002) on a spatial area ("a camera for taking the scanning image…the other camera for taking the reference image" at ¶0004; "an area enclosed by a solid line" at ¶0046 for both the reference and scanning image);

(b) comparing one scan line (R_1 at fig. 9b) in one digital image ("Reference Image" at fig. 9b) of the left and the right digital image with multiple scan lines ($L_1 \ldots L_{64}$ at fig. 9b) in the other digital image ("Scanning Image" at fig. 9b) in a real-time by using a systolic array ("systolic array" at ¶0084; fig. 9; fig. 12) to match each pixel in the one scan line with a pixel in the multiple scan lines ("65th Calculation" at fig. 9b; ¶0084),

wherein said left and right digital images are left and right images of said object ("object" at ¶0005), and wherein matching the pixel in the one scan line with another pixel in the multiple scan lines enables location of the object in said spatial area ("an area enclosed by a solid line" at ¶0046 for both the reference and scanning image) so that imprecision in location and direction of, or distortion caused by, said left and right image acquisition unit is prevented (the purpose of *Oh* is to match the scanning and reference image due to imprecision in location and direction of the two cameras because they are both separate from each other in location and direction; *see* Response to Argument section).

Claim Rejections - 35 U.S.C. § 103

[6] The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

[7] **Claims 3-5** and **7-9** are rejected under 35 U.S.C. 103(a) as being unpatentable over *Oh* in view of U.S. Publication No. 2002/0025075 (published Feb. 28, 2002, hereinafter "Jeong et al.").

Regarding **claim 3**, while *Oh* discloses the apparatus of claim 2, and while *Oh* teaches wherein the multi-layered image matching unit (the processor responsible for execution of fig. 9a; "processor" at ¶0068) includes: a plurality of layers (each layer being what has been calculated (e.g. "To 2nd Strip REG", "To 3rd Strip REG", and so forth)) for receiving the one scan line (R_1 at fig. 9b) in the one digital image ("Reference Image" at fig. 9b) and receiving the multiple scan lines ($L_1 \ldots L_{64}$ at fig. 9b) in the other digital image ("Scanning Image" at fig. 9b) one by one, *Oh* does not disclose wherein two adjacent layers exchange costs and active signals

with each other; and an accumulator for accumulating data fed from the layers to generate the disparity.

Jeong et al. teaches wherein the multi-layered image matching unit (fig. 1, element 13) includes:

wherein two adjacent layers (the two layers as input at fig. 4) exchange costs and active signals with each other (fig. 4, element 44; "matching cost based on a pair of pixels in one scan line of the first and second digital image signals" at ¶0009); and

an accumulator (fig. 4, element 43) for accumulating data fed from the layers to generate the disparity (output at fig. 4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made for the multi-layered image matching unit and systolic array of *Oh* to include wherein two adjacent layers exchange costs and active signals with each other; and an accumulator for accumulating data fed from the layers to generate the disparity as taught by *Jeong et al.* "to provide a real-time stereo image matching apparatus which enables real-time stereo matching, by parallel processing video image sequences using an algorithm which is based on a new trellis based method and is optimal in the Bayesian sense.", *Jeong et al.*, ¶[0008].

Regarding **claim 4**, while *Oh* in view of *Jeong et al.* discloses the apparatus of claim 3, and while *Oh* discloses wherein each of the layers has: a first storing unit (it is inherent if not already implicit that there must be a computer storage/memory of the image for it to be computed at fig. 9b) for storing pixels of the left digital image ("Reference Image" at fig. 9b); and a second storing unit (it is inherent if not already implicit that there must be a computer storage/memory of the image for it to be computed at fig. 9b) for storing pixels of the right

digital image ("Scanning Image" at fig. 9b), *Oh* does not disclose having a plurality of forward processors, stacks and backward processors for generating decision values and the disparity obtained from the left and the right digital image based on a clock signal.

Jeong et al. discloses a apparatus for matching stereo image in real time (fig. 1) that includes wherein each scan line has:

a first storing unit (fig. 1, element 12) for storing pixels of the left digital image ("Lin" at fig. 3);

a second storing unit (fig. 1, element 12) for storing pixels of the right digital image ("Rin" at fig. 3); and

a forward processor (fig. 3, element 30), stack (fig. 3, element 31) and backward processor (fig. 3, element 32) for generating decision values ("decision value" at ¶[0023]) and the disparity ("disparity" at ¶[0023]) obtained from the left and the right digital image based on a clock signal ("Clock" at fig. 3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made for each layer of *Oh* in view of *Jeong et al.* to include having a forward processor, stack and backward processor for generating decision values and the disparity obtained from the left and the right digital image based on a clock signal (thus a plurality of forward processors, stacks and backward processors for all layers) as taught by *Jeong et al.* "to provide a real-time stereo image matching apparatus which enables real-time stereo matching, by parallel processing video image sequences using an algorithm which is based on a new trellis based method and is optimal in the Bayesian sense.", *Jeong et al.*, ¶[0008].

Regarding **claim 5**, while *Oh* in view of *Jeong et al.* disclose the apparatus of claim 4, *Oh* does not teach wherein each of the forward processors of said each of the layers contains: a first multiplexor for determining a minimum cost among a recursive cost within said each of the forward processors and two costs fed from an upper and a lower layer of said each of the layers; a first cost register for storing the minimum cost; an absolute value calculator for calculating as a matching cost a difference between one of the pixels of the first image storing unit and another pixel of the pixels of the second image storing unit; a first adder for adding the matching cost to the minimum cost to generate a first added cost, a second multiplexor for deciding a minimum cost among the first added cost and two costs fed from an upper and a lower forward processor in said each of the layers; a second cost register for storing the minimum cost fed from the second multiplexor, wherein the minimum cost is fed back to the first cost multiplexor as the recursive cost and also provided to the upper and the lower layer; and a second adder for adding the minimum cost stored in the second cost register to an occlusion cost to provide a second added cost to the upper and the lower forward processor.

Jeong et al. discloses a apparatus for matching stereo image in real time (fig. 1) that includes wherein each of the forward processors (fig. 3, element 30; fig. 2, element 22) of each scan line contains:

a first multiplexor (fig.5, element 43) for determining a minimum cost among a recursive cost within said each of the forward processors and two costs fed from an upper and a lower layer of said each scan line (¶¶[0025], [0027]);

a first cost register (fig. 4, element 44) for storing the minimum cost (¶[0025]);

an absolute value calculator (fig. 4, element 41) for calculating as a matching cost a difference between one of the pixels of the first image storing unit and another pixel of the pixels of the second image storing unit (¶[0025]);

a first adder (fig. 4, element 42) for adding the matching cost to the minimum cost to generate a first added cost (¶[0025]),

a second multiplexor (fig. 4, element 43) for deciding a minimum cost among the first added cost and two costs ("Uin2" and "Uin1" at fig. 4) fed from an upper and a lower forward processor in said each of the layers (¶¶[0045], [0046]);

a second cost register (fig. 4, element 44) for storing the minimum cost fed from the second multiplexor, wherein the minimum cost is fed back to the first cost multiplexor as the recursive cost and also provided to the upper and the lower layer (¶[0047]); and

a second adder (fig. 4, element 42) for adding the minimum cost stored in the second cost register to an occlusion cost to provide a second added cost to the upper and the lower forward processor (¶[0045]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made for each layer of *Oh* in view of *Jeong et al.* to include wherein each of the forward processors of said each of the layers contains: a first multiplexor for determining a minimum cost among a recursive cost within said each of the forward processors and two costs fed from an upper and a lower layer of said each of the layers; a first cost register for storing the minimum cost; an absolute value calculator for calculating as a matching cost a difference between one of the pixels of the first image storing unit and another pixel of the pixels of the second image storing unit; a first adder for adding the matching cost to the minimum cost to generate a first

added cost, a second multiplexor for deciding a minimum cost among the first added cost and two costs fed from an upper and a lower forward processor in said each of the layers; a second cost register for storing the minimum cost fed from the second multiplexor, wherein the minimum cost is fed back to the first cost multiplexor as the recursive cost and also provided to the upper and the lower layer; and a second adder for adding the minimum cost stored in the second cost register to an occlusion cost to provide a second added cost to the upper and the lower forward processor as taught by *Jeong et al.* “to provide a real-time stereo image matching apparatus which enables real-time stereo matching, by parallel processing video image sequences using an algorithm which is based on a new trellis based method and is optimal in the Bayesian sense.”, *Jeong et al.*, ¶[0008].

Regarding **claim 7**, *Oh* discloses wherein each of the layers (each layer being what has been calculated (e.g. “To 2nd Strip REG”, “To 3rd Strip REG”, and so forth)) is inputted with pixels (the respective pixels at fig. 9b) of one scan line (R_1 at fig. 9b) of the one digital image (“Reference Image” at fig. 9b) and pixels (the respective pixels at fig. 9b) of multiple scan lines ($L_1 \ldots L_{64}$ at fig. 9b) of the other digital image (“Scanning Image” at fig. 9b).

Regarding **claim 8**, while *Oh* in view of *Jeong et al.* disclose the apparatus of claim 5, *Oh* does not disclose wherein all the cost registers except a 0-th cost register in the forward processors in said each of the layers is initialized with maximum cost, respectively, and the second storing unit is initialized based on the right digital image.

Jeong et al. discloses a apparatus for matching stereo image in real time (fig. 1) that includes wherein all the cost registers except a 0-th cost register in the forward processors in said

each of the layers is initialized with maximum cost, respectively, and the second storing unit is initialized based on the right digital image (¶[0039]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made for each layer of *Oh* in view of *Jeong et al.* to include wherein all the cost registers except a 0-th cost register in the forward processors in said each of the layers is initialized with maximum cost, respectively, and the second storing unit is initialized based on the right digital image as taught by *Jeong et al.* "to provide a real-time stereo image matching apparatus which enables real-time stereo matching, by parallel processing video image sequences using an algorithm which is based on a new trellis based method and is optimal in the Bayesian sense.", *Jeong et al.*, ¶[0008].

Regarding **claim 9**, while *Oh* in view of *Jeong et al.* disclose the apparatus of claim 5, *Oh* does not teach wherein,

if a sum of a processing element number and a forward processing step number is an even number, said each of the forward processors decides a minimum cost among the recursive cost and two added costs obtained by adding the occlusion cost to said two costs fed from the upper and the lower forward processor in said each of the layers, respectively, to provide the minimum cost as a first decision value to a stack,

and, if otherwise, said each of the forward processors determines another minimum cost among a cost obtained by adding an absolute pixel difference of the left and the right digital image to the first decision value and two costs of two forward processors of the upper and the lower layer to provide the minimum cost as a second decision value to the stack.

Jeong et al. discloses a apparatus for matching stereo image in real time (fig. 1) that includes wherein

if a sum of a processing element number and a forward processing step number is an even number, said each of the forward processors decides a minimum cost among the recursive cost and two added costs obtained by adding the occlusion cost to said two costs fed from the upper and the lower forward processor in said each of the layers, respectively, to provide the minimum cost as a first decision value to a stack (¶¶[0036], [0037]; "If i + j is even" and its full condition at ¶[0063]),

and, if otherwise, said each of the forward processors determines another minimum cost among a cost obtained by adding an absolute pixel difference of the left and the right digital image to the first decision value and two costs of two forward processors of the upper and the lower layer to provide the minimum cost as a second decision value to the stack (¶¶[0036], [0037]; "If i + j is odd" and its full condition at ¶[0063]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made for each layer of *Oh* in view of *Jeong et al.* to include wherein, if a sum of a processing element number and a forward processing step number is an even number, said each of the forward processors decides a minimum cost among the recursive cost and two added costs obtained by adding the occlusion cost to said two costs fed from the upper and the lower forward processor in said each of the layers, respectively, to provide the minimum cost as a first decision value to a stack, and, if otherwise, said each of the forward processors determines another minimum cost among a cost obtained by adding an absolute pixel difference of the left and the right digital image to the first decision value and two costs of two forward processors of the

upper and the lower layer to provide the minimum cost as a second decision value to the stack as taught by *Jeong et al.* "to provide a real-time stereo image matching apparatus which enables real-time stereo matching, by parallel processing video image sequences using an algorithm which is based on a new trellis based method and is optimal in the Bayesian sense.", *Jeong et al.*, ¶[0008].

[8] **Claim 15** is rejected under 35 U.S.C. 103(a) as being unpatentable over *Oh* in view of U.S. Patent No. 5,867,591 (issued Feb. 2, 1999, hereinafter "Onda").

Regarding **claim 15**, while *Oh* discloses the apparatus of claim 14, *Oh* does not disclose wherein the step (b) includes the steps of: (b1) determining a path of a minimum cost as a decision value based on pixel data of the one scan line and pixel data of the multiple scan lines; (b2) calculating a disparity from the decision value; and (b3) using the disparity to find a pair of pixels from the left and the right digital image and calculating a distance from the disparity.

Onda discloses wherein the step (b) includes the steps of:

(b1) determining a path of a minimum cost as a decision value ("disp1" and "disp2" at fig. 18; 14:23-31) based on pixel data of the one scan line (pixels in "left window TLk(x,y)" at fig. 17) and pixel data of the multiple scan lines (pixels in "right window TRk(x,y)" at fig. 17; right window at fig. 16, element TR1; 6:29-40);

(b2) calculating a disparity ("identify most-frequent-valued block as true disparity" at fig. 19; Col. 15, lines 35 – 51) from the decision value; and

(b3) using the disparity to find a pair of pixels from the left and the right digital image and calculating a distance from the disparity (once the block disparity is found, the distance between the right and left windows is itself "disp" as shown at fig. 16).

It would have been obvious to one of ordinary skill in the art at the time the invention was made for step (b) of *Oh* to include the steps of: (b1) determining a path of a minimum cost as a decision value based on pixel data of the one scan line and pixel data of the multiple scan lines; (b2) calculating a disparity from the decision value; and (b3) using the disparity to find a pair of pixels from the left and the right digital image and calculating a distance from the disparity as taught by *Onda* "to provide a method of matching stereo images and of detecting disparity between these images, small in the volume of computations, compact in the hardware construction, quick in processing, highly reliable, and excellent in accuracy.", *Onda*, 4:57-61.

Response to Arguments

[9] Remarks/Arguments filed September 3, 2008 with respect to claims 1-15 have been respectfully and fully considered, but not found persuasive.

Remarks regarding claims 1, 2, and 14

> Each of the claims of the present application clearly and explicitly recites multiple scan lines. The Oh publication, on the other hand, clearly does not recite multiple scan lines. As explained in paragraphs [0047] to [0049] of the Oh publication, the image matching means of Oh searches a corresponding pixel or window centered a pixel L(x+d,y) in a scanned image, with respect to a reference pixel or window centered at a pixel L(x,y) in reference image by using Window Matching Count (WMC) values. This search does not involve multiple scan lines, but rather one reference pixel or window centered at L(x,y) in a reference image.

(Applicant Remarks/Arguments at 9, Sep. 3, 2008.)

Examiner's Response

However, *Oh* does disclose multiple scan lines. Scan lines are either rows or columns of the reference or scanning image being used for the calculations of both fig. 9a and 9b, on the assumption that a scan line is more than one pixel. Directing to ¶¶0047-0049 appears misguiding when considering the embodiment of fig. 9a and 9b being used by *Oh* to anticipate the claims in question (¶¶0047-0049 are directed to fig. 1-4). Fig. 9b "65th Calculation" for

example shows reference column item R_1 (a “scan line”) matching up with an array of scanning column items L_{64}-L_1 (“multiple scan lines”). *Oh* supports that a column comprises eleven pixels at ¶0085. The process is repeated for each reference column item until complete, each creating a separate "strip value" later used for matching (*Oh* at ¶0063). Fig. 9b alone is sufficient to meet the “multi-layered image matching unit” of claim 1 (and claim 14 by equivalence).

Furthermore, fig. 12 describes in further detail inputting “[s]imilarities of matched scanning columns, where d=0 63, to a reference column” using a systolic array. *Oh* at ¶0091.

Even if Applicant’s argument is true (one pixel at a time argument), it does not take into account repeating the pixel-step across a plurality of pixels (and thus a "scan line"). The Applicant limiting *Oh* to only disclosing one calculation involving one pixel of the reference image with one other pixel of the scanning image is too specific, as though this may be true it does not consider that "multiple scan lines" exist in the calculations. The Examiner agrees that matching multiple scan lines (as shown in fig. 9) would require it be done pixel by pixel through the processor (as a processor cannot calculate multiple pixels at one specific time but must do each minute calculation one at a time).

Further Remarks regarding claims 1, 2, and 14

> For example, as can be seen in the illustration, the fight digital image might be rotated with respect to the left digital image. Points denoted by [four symbols] are corresponding pixels in the left and fight images, but are in different scan lines. The method of Oh cannot handle this situation, whereas the claimed invention can because it searches multiple scan lines rather than just a single scan line as in the Oh publication.

(Remarks/Arguments at 9.)

Examiner’s Response

However, the Examiner stresses more definite language in the claim in what specifically the process of Applicant's invention is doing such that "Oh cannot handle this situation [as can be seen in the illustration]".

Remarks regarding claims 3-5, 7-9, and 15

> This rejection is again respectfully traversed on the grounds that the Jeong publication, like the Oh publication, fails to disclose or suggest matching of each pixel in one scan line with another pixel in multiple scan lines, as claimed. The Jeong publication merely discloses left and fight image conversion and not the claimed exchange of information between two adjacent processing elements, much less the claimed matching between single and multiple scan lines.
>
> …
> This rejection is also again respectfully traversed on the grounds that the Onda publication, like the Oh publication, fails to disclose or suggest matching of each pixel in one scan line with another pixel in multiple scan lines using a systolic array, as claimed. As mentioned in the previous response, the Onda patent is totally silent on use of a systolic array having processing elements which can exchange information with two adjacent processing elements. Further, the image matching means of Onda only determines a similarity evaluation value between a left window and a fight window, and does not search of a pixel in the right window to correspond to each pixel in the left window, as in the claimed invention.

(<u>Remarks/Arguments</u> at 10.)

Examiner's Response

However, *Oh* does disclose multiple scan lines as thus the question of whether the secondary references fail to disclose or suggest the matching of each pixel in one scan line with another pixel in multiple scan lines is irrelevant.

Allowable Subject Matter

[10] **Claims 6** and **10-13** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

[11] The following is a statement of reasons for the indication of allowable subject matter:

Regarding **claim 6**, while the prior art teaches claim 1-4 (*see* prior art rejections above), the prior art does not teach wherein each of the backward processors of said each of the layers includes: an OR gate for logically summing two active bit paths inputted from an upper and a lower backward processor in said each of the layers, two active bit paths inputted from an upper and a lower layer of said each of the layers and a recursive active bit path within said each of the backward processors to generate a logical sum of five active bit paths; an activation register for storing the logical sum of five active bit paths; a demultiplexor for demultiplexing the logical sum of five active bit paths based on a decision value fed from the stack; and a tri-state buffer for outputting the decision value in case the logical sum of five active bit paths in the activation register is high.

Conclusion

[12] Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 C.F.R. 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

[13] Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID P. RASHID whose telephone number is (571)270-1578. The examiner can normally be reached Monday - Friday 7:30 - 17:00 ET.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vikkram Bali can be reached on (571) 272-74155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) apparatus. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR apparatus, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR apparatus, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information apparatus, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/David P. Rashid/
Examiner, Art Unit 2624

David P Rashid
Examiner
Art Unit 26244

/Vikkram Bali/

Supervisory Patent Examiner, Art Unit 2624